REMARKS/ARGUMENTS

Examiner:

Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which applicant regards as the invention.

Response:

Claims 1-14 and 16-22 have been amended utilizing special care in an effort to comply with each and every Examiner cited example as well as additional examples of indefinite and function or operational language questions.

Amendments to claims are supported by the Paragraph beginning with the words "Please refer to Fig.5" on Line 27 of Page 6, the Paragraph beginning with the words "Please refer to Fig.6a" on Line 21 of Page 8, Fig.6a, and corresponding original claims. No new material has been introduced. The Applicant believes that claims 1-22 as amended fully comply with the requirements of 35 U.S.C. 112, second paragraph, and respectfully request reconsideration of all claims under this rejection.

Examiner:

Claims 1, 10, and 17, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by the Scott et al. reference (U.S. Patent 6,369,661).

Response:

Scott et al. does disclose frequency splitting using an interpolation method, but teaches a switch for selecting first and second output signals generated by a ring oscillator. A current splitter is utilized for splitting a current of each of selected first and second signals into a plurality of intermediate signals, a set of weight switches are used for selecting from the intermediate signals; and currents of selected intermediate signals are selectively summed to generate a current of a selected phase (Col.6, line 31 – Col.7, line 10).

As such, it is believed that the Scott et al. reference fails to anticipate the present invention because the details are quite different from the current invention. For example, the switch prevents it from generating a plurality of output clocks simultaneously, and because the frequency of the output clocks is the same as the frequency of the inputted signal, cannot address the applications prior art problem of using a reduced number of inverters in the ring oscillator to reduce power consumption and improve stability. Merely adding a frequency divider to Scott et al. will not solve this problem.

The present invention does not selectively sum currents. Rather, the rising and/or falling edges of a plurality of periods of a reference clock is used to trigger one rising or falling edge of the output clock. The difference between selectively summing currents and the method of the present invention can be clearly seen by comparing the current application's Fig.2 with Fig.6a. By utilizing a plurality of reference clock periods to generate a single period of the output clock, the desired phase difference can be generated while achieving the stated goal of reducing instability and jitters found in prior art reference clocks by reducing the number of invertors in the ring oscillator (Page 22,

Line 24 – Page 23, Line 23).

As amended, it is believed that independent claims 1, 10, and 17 each comprise the above-described limitation of generating the output clock having a period equal to a plurality of periods of the reference clock. Therefore, the Applicant believes that the present application as currently claimed represents a new and useful device not taught or anticipated by known prior art and respectfully requests reconsideration and allowance of claims 1, 10, and 17.

Respectfully submitted,

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Note: Please leave a message in my voice mail if you need to talk to me. The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan).